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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/652,619	08/31/2000	Gurtej Singh Sandhu	303.085US4	4342

21186 7590 04/26/2002

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EXAMINER

BERRY, RENEE R

ART UNIT	PAPER NUMBER
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2818

DATE MAILED: 04/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/652,619

Applicant(s)

Sandhu et al.

Examiner

Renee Berry

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on _____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 21-31 and 55-99 is/are pending in the application.
- 4a) Of the above, claim(s) 55-90 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 21-31 and 91-99 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- a) ☐ All b) ☐ Some* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892) 18) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 19) ☐ Notice of Informal Patent Application (PTO-152)
- 17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____ 20) ☐ Other: _____

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DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group I in Paper No. 7 is acknowledged.
2. Claims 55-90 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 7.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 21-31 and 91-99 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent no. 6,369,430 to Adetutu et al. in view of US patent no. 6,143,593 to Augusto.

In regard to claims 21 and 91, Adetutu teaches an integrated circuit having a substrate; a first layer of material formed on the substrate (silicate glass oxide/BPSG), the first layer having contact vias extending through to the substrate; a second layer formed on the first layer, the

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second layer lining the contact vias; and a metallization layer on the second layer at column 3, lines 34-38 and column 4, lines 13-20.

In regard to claims 22 and 26, Adetutu teaches the metallization layer comprises non-alloy copper at column 4, lines 15-18.

In regard to claim 23, Adetutu teaches the metallization layer fills the contact vias .

In regard to claim 24, Augusto teaches the first layer has a first surface potential and the second layer has a second surface potential, and wherein the first surface potential is lower than the second surface potential.

In regard to claim 27, Adetutu teaches the first layer comprises poly-silicon and the second layer comprises titanium nitride at column 2, lines 45-50.

In regard to claim 95, Adetutu teaches the second layer includes titanium nitride at column 4, lines 6-12.

In regard to claim 97, Adetutu teaches the first layer and the second layer have a thickness on the order of 100 to 500 Angstroms at column 3, lines 30-33.

However, Adetutu does not teach the first layer has a first surface voltage, the second layer has a second surface voltage, and the first surface voltage is lower than the second surface voltage.

In regard to claim 25, Augusto teaches an integrated circuit having a substrate; a first layer of material formed on the substrate, the first layer having a first surface voltage; a second layer of material formed on the first layer, the second layer having a second surface voltage, the second

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surface voltage being different than the first surface voltage; and a metallization layer formed on the second layer.

In regard to claim 28, Augusto teaches the first surface voltage is lower than the second surface voltage at column 17, lines 1-22.

In regard to claim 29, Augusto teaches an integrated circuit having a substrate; a first layer of material formed on the substrate; a first layer of formed on the substrate; an insulator layer formed on the first layer, the insulator layer and the first layer having contact vias; a second layer formed on the first layer, the second layer lining the contact vias; and a metallization layer on the second layer at column 17, lines 1-22.

In regard to claim 30, Augusto teaches the metallization layer on the second layer fills the contact vias at column 12, lines 10-16, figure 23, ref # 76.

In regard to claim 31, Augusto teaches the first layer and the second layer have exposed surfaces upon which voltage may be applied at column 17, lines 1-22.

In regard to claim 92, Augusto teaches the first layer of material includes doped polysilicon at column 14, lines 31-35.

In regard to claim 93, Augusto teaches the first layer of material includes undoped polysilicon at column 14, lines 31-35.

In regard to claim 96, Augusto teaches the second layer includes a barrier layer material at column 12, lines 5-11.

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In regard to claim 99, Augusto teaches the first layer has a first surface voltage, the second layer has a second surface voltage, and the first surface voltage is lower than the second surface voltage at column 17, lines 1-22.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified Adetutu to include the first layer has a first surface voltage, the second layer has a second surface voltage, and the first surface voltage is lower than the second surface voltage, since such a modification would result in an improved charge carrier mobility of the channel films, as described in column 4, lines 20-25 of Augusto.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to R. R. Berry whose telephone number is (703) 305-4544.


RRB

April 22, 2002


HOAI HO
PRIMARY EXAMINER